ISSN: 2277-9655
Scientific Journal Impact Factor: 3.449
(ISRA), Impact Factor: 2.114

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

Efficient Design Of 4-Bit Binary Adder Using Reversible Logic Gates

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Abstract

This paper proposes the design of 4-bit adder and implementation of adder Reversible logic gate to improve the design in terms of garbage outputs and delay. In the recent years, reversible logic has emerged as a promising technology having its applications in low power CMOS, quantum computing, nanotechnology and optical computing because of it's zero power dissipation under ideal conditions. Thus, the project will provide the reversible logic implementation of the conventional 4-bit adder using Toffoli gate, Peres gate and using both Peres gate and Fredkin gate. The proposed reversible logic implementation of the 4- bit adder is optimized to obtain minimum number of logic gates and garbage outputs. This project work on the reversible 4-bit adder circuits designed and proposed here form the basis of the decimal ALU of a primitive quantum CPU. The designed and optimized 4-bit reversible adder is implemented in VHDL Using Xilinx ISE 12.1 tool.

Keywords: Reversible logic, Feynman gate, Fredkin Gate, Toffoli Gate, Peres Gate.

Introduction

The Power dissipation is one of the most important factors in VLSI circuit design. Due to the information loss in irreversible hardware computation, it results in energy dissipation. Part of the energy dissipation is due to the non-identity of switches. Because of higher level of integration and use of new fabrication process have dramatically reduced the heat loss over last decades [5]. Other part of the energy dissipation is according to Landauer's research, the amount of energy dissipated for every irreversible bit operation is at least KTln2 joules. Where K is the Boltzmann's constant and T is the temperature at which operation is performed [1].

In 1973, Bennett showed that KTln2 energy would not be dissipated from a system as long as the system allows the reproduction of the inputs from which does not result in information called reversible [2].

Reversible are circuit (gates) in which one to one mapping between inputs and outputs. Reversible logic supports the process of running the systems both forward and backward [3]. The amount of energy dissipation in a system increases in direct proportion to the number of bits that are erased during computation. Bennett showed that KTln2 energy dissipation would not occur, if a computation is performed in a reversible way. Reversible computation in a system can be performed if the system is composed of reversible gates. The current irreversible technologies will dissipate a lot of heat and can reduce the life of the circuit [4]. The reversible logic operations do not erase (lose) information and dissipate very less heat. Thus, reversible logic is likely to be in demand in high speed power aware circuits. Minimum number of gates is used for implementation

- Restrict the number of garbage outputs as fewer as possible
- Design should cater all the good features of reversible logic synthesis

This project focuses on the design and optimization of 4-bit adder and implement adder using reversible gates.

Need of reversible circuits

Following are the need of reversible circuits:

- The amount of heat dissipation due to information loss in irreversible circuit is avoided by reversible logic gates.
- Reversible logic circuits are in demand for high speed power aware circuits.
- Reversible logic gates are needed to recover the state of inputs from outputs.
- Reversible computing will lead to improvement in energy efficiency.

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- Energy efficiency will fundamentally affect the speed of circuits such as nano circuits and therefore the speed of most computing applications.
- High performance chips are releasing large amounts of heat, to reduce the heat reversible logic gates are used.

Reversible gates used for designing

Feynman Gate

Feynman gate is a 2*2 one through reversible gate as shown in figure 1. The input vector is I(A, B) and the output vector is O(P, Q). The outputs are defined by P=A, Q=A ⊕ B. Quantum cost of a Feynman gate is 1.[6].

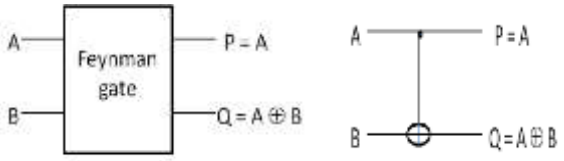

Figure 1: Feynman Gate

Fredkin Gate

Figure 2 shows a 3*3 Fredkin gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A′B⊕ AC and R=A′C⊕ AB. Quantum cost of a Fredkin gate is 5 [7].

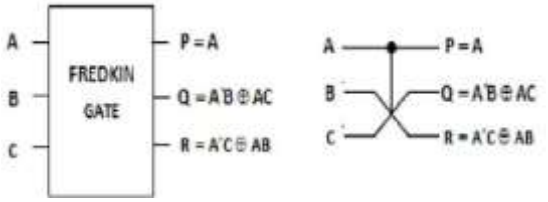

Figure 2: Fredkin Gate

Toffoli Gate

Figure 3 shows a 3*3 Toffoli gate. The input vector is I (A, B, C) and the output vector is O(P,Q,R). The outputs are defined by P=A, Q=B, R=AB⊕C. Quantum cost of a Toffoli gate is 5 [8].

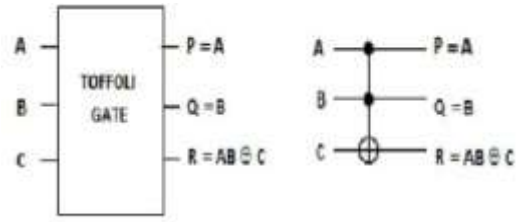

Figure 3: Toffoli Gate

Peres Gate

Figure 4 shows a 3*3 Peres gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = A⊕B and R=AB⊕C. Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost [9].

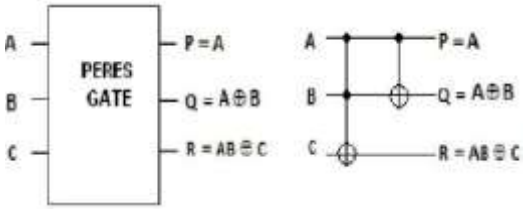

Figure 4: Peres Gate

Synthesis of reversible circuits

The main difference of synthesizing a circuit with reversible gates as compared to the standard conventional circuits is the following

- The number of outputs of a logic gate is equal to the number of inputs
- Every gate output which is not used as input for a next gate or not used as a primary output is called as Garbage. If the output is left unattended or if the mirror circuit and spy gates are added.
- In reversible logic, outputs from one gate can be used as inputs to the next gate without fan-out of more than one.

Applications of reversible circuits

The most prominent application of reversible logic lies in,

- Quantum computers
- Low power CMOS design
- Optical computing
- Nanotechnology

Reversible logic implementation of 4 –bit binary adder using full adder circuit

A 4-bit binary adder is a digital circuit that produces the arithmetic sum two 4-bit numbers. It can be constructed with full adders connected in cascade, with the output carry from each full adder connected to input carry of the next full adder in the chain. Figure 5 shows the interconnection of 4 full adder (FA) circuits to provide a 4-bit binary adder. The carries are connected in a chain through the full adders. The input carry to the adder is C_{in}, and it ripples though the full adders to the output carry C_{out}. The ∑ outputs generate the required sum bits. It can

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Scientific Journal Impact Factor: 3.449
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be used in many applications involving arithmetic operations.

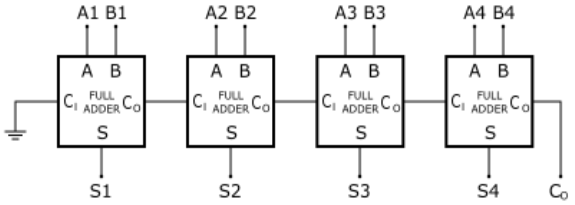

Figure 5: 4-bit Conventional binary adder circuit

Proposed design: reversible logic implementation of full adder circuit

Case 1: using only peres gate

Full adder is the fundamental building block in many computational units. The full adder circuit's output is given by the following equations:

Sum=A⊕B⊕C

Cout= (A⊕B) C+AB

The reversible logic implementation of full-adder circuit and other adder circuits and their minimization issues has been discussed in [10-13]. In this case the full adder is designed by using five 3*3 Peres gates only (shown in figure 6). Here the number of constant inputs is 5 and the number of garbage outputs is 8. So the 4-bit binary adder (using only Peres gate) having 5*4=20 constant inputs and 8*4=32 garbage outputs.

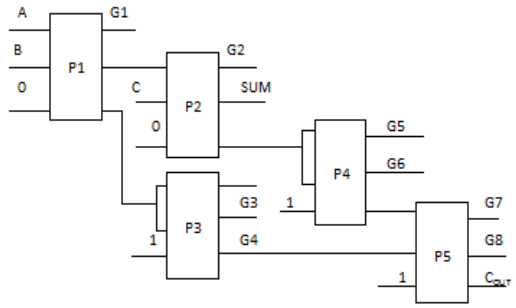

Figure 6: Reversible full adder circuit (by using only Peres gate)

Case 2: using only toffoli gate

The reversible logic implementation of full-adder circuit using only Toffoli gate. In this case the full adder is designed by using seven 3*3 Toffoli gates only (shown in figure 7). Here the number of constant inputs is 7 and the number of garbage outputs is 14. So the 4-bit binary adder (using only Toffoli gate) having 7*4=28 constant inputs and 14*4=56 garbage outputs.

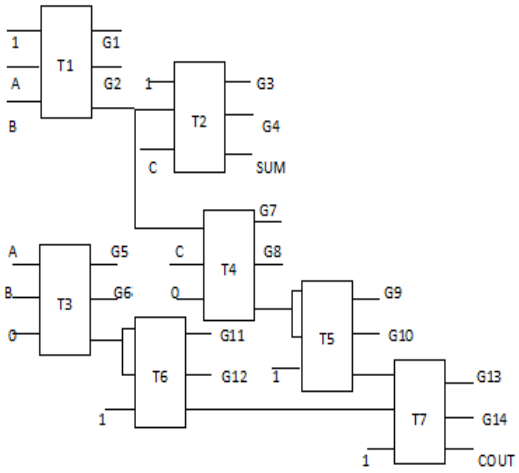

Figure 7: Reversible full adder circuit (by using only Toffoli gate)

Case 3: using only peres gate and fredkin gate

The reversible logic implementation of full-adder circuit using both Peres gate and Fredkin gate. In this case the full adder is designed by using two 3*3 Peres gates and one 3*3 Fredkin gate (shown in figure 8). This implementation of reversible full adder circuit is also efficient in terms of gate count, garbage outputs and constant input than the existing counter parts.

Here the number of constant inputs is 3 and the number of garbage outputs is 4. So the4-bit binary adder (using only Peres gate) having 3*4=12 constant inputs and 4*4=16 garbage outputs.

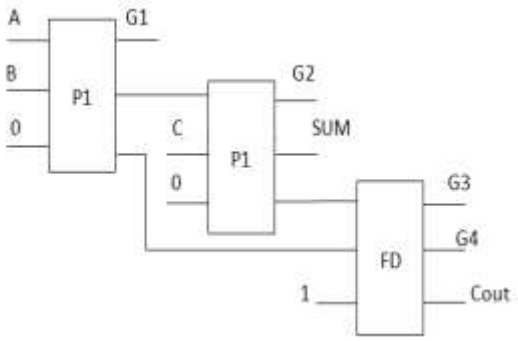

Figure 8: Reversible full adder circuit (by using Peres gate and Fredkin gate)

Results and discussion

The following demonstrates that the proposed reversible full adder gate is superior to the existing counterparts in terms of hardware complexity, garbage outputs and constant inputs.

Let

a = A two input EX-OR gate calculation

ISSN: 2277-9655
Scientific Journal Impact Factor: 3.449
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b = A two input AND gate calculation
c = A two input NAND gate calculation
d = A two input OR gate calculation
T = Total logical calculation

Tables:

Table 1.
Comparative experimental results of different reversible 4-bit binary adder

Reversible 4-bit binary adder	Constant inputs	Garbage outputs	Total no. of gates	Total logical calculation	Delay (in ns)
Case 1	20	32	20	8a+8b+12c	10.587
Case 2	28	56	28	8a+8b+12c	10.587
Case 3	12	16	12	8a+8b+4d	10.487

Conclusion

As per the observation of three cases of adder circuits using the reversible logic, the case 3 which uses only the Peres and Fredkin gate has more flexible and less complex operational with high speed. Hence, it more efficient as compared to all cases.

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ISSN: 2277-9655
Scientific Journal Impact Factor: 3.449
(ISRA), Impact Factor: 2.114

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